ESE 345 Spring 2021

Computer Architecture

1. Course Staff and Office Hours

Instructor: Mikhail Dorojevets
Mikhail.Dorojevets@stonybrook.edu
243 Light Engineering

Course website: http://www.ece.stonybrook.edu/~midor/ESE345/index.html

Lectures: MW 6:05-7:25 PM online **by Skype Conference call**
Office Hours: online **by Skype** on Monday, 10:00 am –12:00 pm (students need to request a time slot in advance)
Other hours by appointment

TAs:

Xiaokun Zhao (course subject and **homeworks**)
Email: xiaokun.zhao@stonybrook.edu
TA hours: Friday 2:00-3:00 pm **by Skype**

Ryan Thielke (course subject and **a project**)
Email: ryan.thielke@stonybrook.edu
TA hours: Tuesday 2:00-3:00 pm **by Skype**

Office hours may change. Please check the course website http://www.ece.stonybrook.edu/~midor/ESE345/index.html *for most up-to-date information.*

2. Course Description

This course focuses on the fundamental techniques of designing and evaluating modern computer architectures and tradeoffs present at the hardware/software boundary. The emphasis is on instruction set design, processor design, memory and parallel processing. Students will undertake a design project using a hardware description language and modern CAD tools.

Prerequisites: ESE 280 and ESE 382

Credits: 3

3. Textbook

David A. Patterson and John L. Hennessy "Computer Organization & Design The Hardware/Software Interface," Fifth Edition by David A. Patterson and John L. Hennessy, 2014 by Elsevier Inc. ISBN:978-0-12-407726-3

4. Course Learning Objectives

To give students in-depth understanding of modern digital computer systems and tradeoffs present at the hardware-software interface. Based on that knowledge, they will be able to design principal processor components by applying the following design steps: definition of an instruction set architecture, cost/performance trade-offs, and gate-level and VHDL/Verilog design and implementation with modern CAD tools.

5. Student Learning Outcomes

Upon completion of this course, students will learn: 1) computer performance and instruction set design principles, 2) MIPS architecture and basics of assembly language programming, 3) integer and floating-point arithmetic, 4) processor, caches, and memory design, and 5) use of VHDL/Verilog languages in the processor design and verification.

	Student Outcomes	% contribution
1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.	70
2	an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.	30
3	an ability to communicate effectively with a range of audiences.	
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgements, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.	

5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.	
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgement to draw conclusions.	
7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.	

6. Schedule

The lectures will be held twice a week for 1 hour and 20 minutes each.

Week 1.	Introduction, technology overview, history of digital computers, instruction set architectures
Week 2.	Computer performance, and introduction to the MIPS architecture
Week 3.	MIPS operations and assembly-language programming
Week 4.	Adders, multipliers, dividers, and shifters
Week 5.	Floating point arithmetic: add and multiply.
Week 6.	*Midterm 1*. Design process, register transfer, single cycle datapath and control
Week 7.	Multiple cycle processor and multicycle controller
Week 8.	Pipelining
Week 9.	Pipelined processor datapath and control
Week 10.	Introduction to memory systems and SRAM/DRAM technology
Week 11.	Cache design
Week 12.	Virtual memory, translation look-aside buffers
Week 13.	Review of multithreaded and multimedia processors. *Project presentations*.

7. Assignments

7.1. Homework Assignments

Homework Assignments will be issued roughly bi-weekly. A schedule will be available on the class website.

All homework assignments must be submitted to **TA Xiaokun Zhao by email**.

7.2. Project

Project Part 1 (VHDL ALU functions) Deadline: 11:59 PM **March 28**, 2021 by email to **TA Ryan Thielke** and Instructor

Full Project Deadline: Monday, 11:59 PM **May 3**, 2021 by email to **TA Ryan Thielke** and Instructor

7.3. Collaboration Policy

Homework assignments are to be completed individually. You may *discuss* them with your classmates. However, you must write up your own solution individually without any help from any other person.

8. Grading

Your grade will be based on homework assignments, two midterm exams, and a project.

Homework Assignments	12%
Midterm Exam 1	33%
Midterm Exam 2	33%
Project	22%

Submissions of both midterms & project are <u>required</u> for every student in this class!

9. Academic Honesty

Any academic dishonesty on a written homework or lab will result in a zero grade for the assignment for all parties involved.

All exam work must be entirely your own with no collaboration or outside materials/information. Any academic dishonesty on the midterm exams or the project will result in failing the course. The case will be submitted to the College of Engineering's Committee on Academic Standing and Appeals.

10. Electronic Communication Statement

Email and **Skype** are the ways the faculty and TA officially communicate with you for this course. It is your responsibility to make sure that you have your email in your official University email account **<u>and your personal Skype account</u>**. **You need to email your Skype Name to Instructor or contact Instructor by Skype before the semester starts to be included into a Skype group for the class**. For most students an official University email account is Google Apps for Education (http://www.stonybrook.edu/mycloud), but you may verify your official Electronic Post Office (EPO) address at http://it.stonybrook.edu/help/kb/checking-or-changing-your-mail-forwarding-address-in-the-epo.

If you choose to forward your official University email to another off-campus account, faculty are not responsible for any undeliverable messages to your

alternative personal accounts. You can set up Google Mail forwarding using these DoIT-provided instructions found at http://it.stonybrook.edu/help/kb/setting-up-mail-forwarding-in-google-mail.

If you need technical assistance, please contact Client Support at (631) 632-9800 or supportteam@stonybrook.edu.

11. Student Accessibility Support Statement

If you have a physical, psychological, medical, or learning disability that may impact your course work, please contact the Student Accessibility Support Center, 128 ECC Building, (631) 632-6748, or at sasc@stonybrook.edu. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

12. Academic Integrity Statement

Each student must pursue their academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

13. Critical Incident Management Statement

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of University Community Standards any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures. Further information about most academic matters can be found in the Undergraduate Bulletin, the Undergraduate Class Schedule, and the Faculty-Employee Handbook.